

1. A differential pixel for an imager device, said pixel comprising:
 - a plurality of photosensors;
 - a plurality of transfer transistors, each transfer transistor connected to and transferring charge from a respective photosensor;
 - a plurality of storage nodes, each node being coupled to a respective transfer transistor and storing charge transferred by a respective one of said plurality of photosensors; and
 - a differential amplifier connected to said storage nodes and outputting a plurality of differential signals for each photosensor.
2. The pixel of claim 1 further comprising a row select transistor connected between a current source and said differential amplifier, said row select transistor causing said current source to be connected to said amplifier when activated.
3. The pixel of claim 2, wherein said current source is a tail current source.
4. The pixel of claim 1, wherein said amplifier is coupled to a plurality of output lines.
5. The pixel of claim 4, wherein said output lines are electrically coupled to respective loads.
6. The pixel of claim 1, wherein said differential amplifier comprises two source follower transistors, each source follower transistor having a gate terminal connected to a respective storage node, a

first source/drain terminal connected to an output line, and a second source/drain terminal connected to a second node.

7. The pixel of claim 6 further comprising:

a row select transistor; and

a current source, said row select transistor being coupled between said second node and said current source, said row select transistor causing the current source to be connected to said second node when activated.
8. The pixel of claim 7, wherein said current source is a tail current source.
9. The pixel of claim 7 further comprising a plurality of reset transistors, each reset transistor being coupled between a reset voltage source and a respective storage node, said reset transistors being activated by a shared reset control signal such that each reset transistor is activated at a same time.
10. The pixel of claim 1, wherein said plurality of transfer transistors are activated in sequence such that charges from said plurality of photosensors are transferred to said amplifier in a sequential manner.
11. The pixel of claim 1 further comprising a plurality of reset transistors, each reset transistor being coupled between a reset voltage source and a respective storage node, said reset transistors being activated

by a shared reset control signal such that each reset transistor is activated at a same time.

12. The pixel of claim 11, wherein said differential amplifier outputs a first differential signal on a first output line, said first differential signal comprising a difference between a plurality of reset voltage signals input from said storage nodes.
13. The pixel of claim 12, wherein said differential amplifier outputs a second differential signal on the first output line, said second differential signal comprising a difference between a pixel voltage signal input from a first storage node and a reset voltage signal input from a second storage node.
14. The pixel of claim 12, wherein said differential amplifier outputs a second differential signal on a second output line, said second differential signal comprising a difference between a plurality of reset voltage signals input from said storage nodes.
15. The pixel of claim 14, wherein said differential amplifier outputs a third differential signal on the second output line, said third differential signal comprising a difference between a pixel voltage signal input from a first storage node and a reset voltage signal input from a second storage node.
16. The pixel of claim 1, wherein a number of photosensors is two.
17. The pixel of claim 1, wherein a number of photosensors is more than two.

18. The pixel of claim 1, wherein said plurality of differential signals comprises a plurality of differential reset signals and a plurality of differential pixel signals.
19. A differential pixel for an imager device, said pixel comprising:
 - a plurality of photosensors;
 - a plurality of storage nodes, each node being coupled to and storing charge from a respective one of said plurality of photosensors; and
 - a differential amplifier connected to said storage nodes and outputting a plurality of differential signals for each photosensor.
20. The pixel of claim 19 further comprising a row select transistor connected between a current source and said differential amplifier, said row select transistor causing said current source to be connected to said amplifier when activated.
21. The pixel of claim 19, wherein said amplifier is coupled to a plurality of output lines.
22. The pixel of claim 21, wherein said output lines are electrically coupled to respective loads.
23. The pixel of claim 19, wherein said differential amplifier comprises two source follower transistors, each source follower transistor having a gate terminal connected to a respective storage node, a first source/drain terminal connected to an output line, and a second source/drain terminal connected to a second node.

24. The pixel of claim 19 further comprising a plurality of reset transistors, each reset transistor being coupled between a reset voltage source and a respective storage node, said reset transistors being activated by a shared reset control signal such that each reset transistor is activated at a same time.
25. The pixel of claim 24, wherein said differential amplifier outputs a first differential signal on a first output line, said first differential signal comprising a difference between a plurality of reset voltage signals input from said storage nodes.
26. The pixel of claim 25, wherein said differential amplifier outputs a second differential signal on the first output line, said second differential signal comprising a difference between a pixel voltage signal input from a first storage node and a reset voltage signal input from a second storage node.
27. The pixel of claim 25, wherein said differential amplifier outputs a second differential signal on a second output line, said second differential signal comprising a difference between a plurality of reset voltage signals input from said storage nodes.
28. The pixel of claim 27, wherein said differential amplifier outputs a third differential signal on the second output line, said third differential signal comprising a difference between a pixel voltage signal input from a first storage node and a reset voltage signal input from a second storage node.

29. The pixel of claim 19, wherein said plurality of differential signals comprises a plurality of differential reset signals and a plurality of differential pixel signals.
30. An imager device comprising:
- a plurality of differential pixels organized as an array having rows and columns;
 - a plurality of output lines coupled to said differential pixels, each pixel outputting differential reset signals and differential pixel signals on a respective output line.
31. The imager device of claim 30, further comprising a plurality of row select transistors, each of said row select transistors being connected between a current source and a respective row of differential pixels, each row select transistor causing its respective current source to be connected to its respective row when activated.
32. The imager device of claim 31, wherein said current source is a tail current source.
33. The imager device of claim 30, wherein each differential pixel comprises:
- a plurality of photosensors;
 - a plurality of transfer transistors, each transfer transistor connected to and transferring charge from a respective photosensor;

a plurality of storage nodes, each node being coupled to a respective transfer transistor and storing charge transferred by a respective one of said plurality of photosensors; and

a differential amplifier connected to said storage nodes and outputting a plurality of differential signals for each photosensor.

34. The imager device of claim 33, wherein said amplifier is coupled to a respective plurality of output lines.

35. The imager device of claim 34, wherein said output lines are electrically coupled to respective loads.

36. The imager device of claim 33, wherein said differential amplifier comprises two source follower transistors, each source follower transistor having a gate terminal connected to a respective storage node, a first source/drain terminal connected to an output line, and a second source/drain terminal connected to a second node.

37. The imager device of claim 36 further comprising:

a row select transistor; and

a current source, said row select transistor being coupled between said second node and said current source, said row select transistor causing the current source to be connected to said second node when activated.

38. The imager device of claim 37 further comprising a plurality of reset transistors, each reset transistor being coupled between a reset voltage source and a respective storage node, said reset transistors

being activated by a shared reset control signal such that each reset transistor is activated at a same time.

39. The imager device of claim 33, wherein said plurality of transfer transistors are activated in sequence such that charges from said plurality of photosensors are transferred to said amplifier in a sequential manner.
40. The imager device of claim 33 further comprising a plurality of reset transistors, each reset transistor being coupled between a reset voltage source and a respective storage node, said reset transistors being activated by a shared reset control signal such that each reset transistor is activated at a same time.
41. The imager device of claim 40, wherein said differential amplifier outputs a first differential signal on a first output line, said first differential signal comprising a difference between a plurality of reset voltage signals input from said storage nodes.
42. The imager device of claim 41, wherein said differential amplifier outputs a second differential signal on the first output line, said second differential signal comprising a difference between a pixel voltage signal input from a first storage node and a reset voltage signal input from a second storage node.
43. The imager device of claim 41, wherein said differential amplifier outputs a second differential signal on a second output line, said second differential signal comprising a difference between a plurality of reset voltage signals input from said storage nodes.

44. The imager device of claim 43, wherein said differential amplifier outputs a third differential signal on the second output line, said third differential signal comprising a difference between a pixel voltage signal input from a first storage node and a reset voltage signal input from a second storage node.
45. A processor system comprising:
- an imager device comprising:
- a plurality of differential pixels organized as an array having rows and columns;
- a plurality of output lines coupled to said differential pixels, each pixel outputting differential reset signals and differential pixel signals on a respective output line.
46. The system of claim 45, wherein said imager device further comprises a plurality of row select transistors, each of said row select transistors being connected between a current source and a respective row of differential pixels, each row select transistor causing its respective current source to be connected to its respective row when activated.
47. The system of claim 46, wherein said current source is a tail current source.
48. The system of claim 45, wherein each differential pixel comprises:
- a plurality of photosensors;

- a plurality of transfer transistors, each transfer transistor connected to
and transferring charge from a respective photosensor;
- a plurality of storage nodes, each node being coupled to a respective
transfer transistor and storing charge transferred by a respective
one of said plurality of photosensors; and
- a differential amplifier connected to said storage nodes and outputting a
plurality of differential signals for each photosensor.
49. The system of claim 48, wherein said amplifier is coupled to a
respective plurality of output lines.
50. The system of claim 49, wherein said output lines are electrically
coupled to respective loads.
51. The system of claim 48, wherein said differential amplifier comprises
two source follower transistors, each source follower transistor
having a gate terminal connected to a respective storage node, a
first source/drain terminal connected to an output line, and a
second source/drain terminal connected to a second node.
52. The system of claim 51, wherein said imager device further
comprises:
- a row select transistor; and
- a current source, said row select transistor being coupled between said
second node and said current source, said row select transistor
causing the current source to be connected to said second node
when activated.

53. The system of claim 52, wherein said imager device further comprises a plurality of reset transistors, each reset transistor being coupled between a reset voltage source and a respective storage node, said reset transistors being activated by a shared reset control signal such that each reset transistor is activated at a same time.
54. The system of claim 53, wherein said plurality of transfer transistors are activated in sequence such that charges from said plurality of photosensors are transferred to said amplifier in a sequential manner.
55. The system of claim 53, wherein said imager device further comprises a plurality of reset transistors, each reset transistor being coupled between a reset voltage source and a respective storage node, said reset transistors being activated by a shared reset control signal such that each reset transistor is activated at a same time.
56. The system of claim 48, wherein said differential amplifier outputs a first differential signal on a first output line, said first differential signal comprising a difference between a plurality of reset voltage signals input from said storage nodes.
57. The system of claim 56, wherein said differential amplifier outputs a second differential signal on the first output line, said second differential signal comprising a difference between a pixel voltage signal input from a first storage node and a reset voltage signal input from a second storage node.

58. The system of claim 56, wherein said differential amplifier outputs a second differential signal on a second output line, said second differential signal comprising a difference between a plurality of reset voltage signals input from said storage nodes.
59. The system of claim 58, wherein said differential amplifier outputs a third differential signal on the second output line, said third differential signal comprising a difference between a pixel voltage signal input from a first storage node and a reset voltage signal input from a second storage node.
60. A method of operating a differential image pixel circuit, said method comprising:
- simultaneously resetting two photosensors;
- outputting a first differential signal corresponding to a difference between reset signals associated with the two reset photosensors;
- transferring a first photo-generated charge from a first of the two photosensors to a first storage node; and
- outputting a second differential signal corresponding to a difference of a signal associated with the transferred first charge and a reset signal associated with a second of the two photosensors.
61. The method of claim 60, further comprising the step of using the first and second differential signals to obtain a correlated double sampled signal.
62. The method of claim 60 further comprising the steps of:

- outputting a third differential signal corresponding to a difference between reset signals associated with the two reset photosensors;
- transferring a second photo-generated charge from the second of the two photosensors to a second storage node; and
- outputting a fourth differential signal corresponding to a difference of a signal associated with the transferred second charge and a reset signal associated with the first of the two photosensors.
63. The method of claim 62, further comprising the step of using the third and fourth differential signals to obtain a correlated double sampled signal.